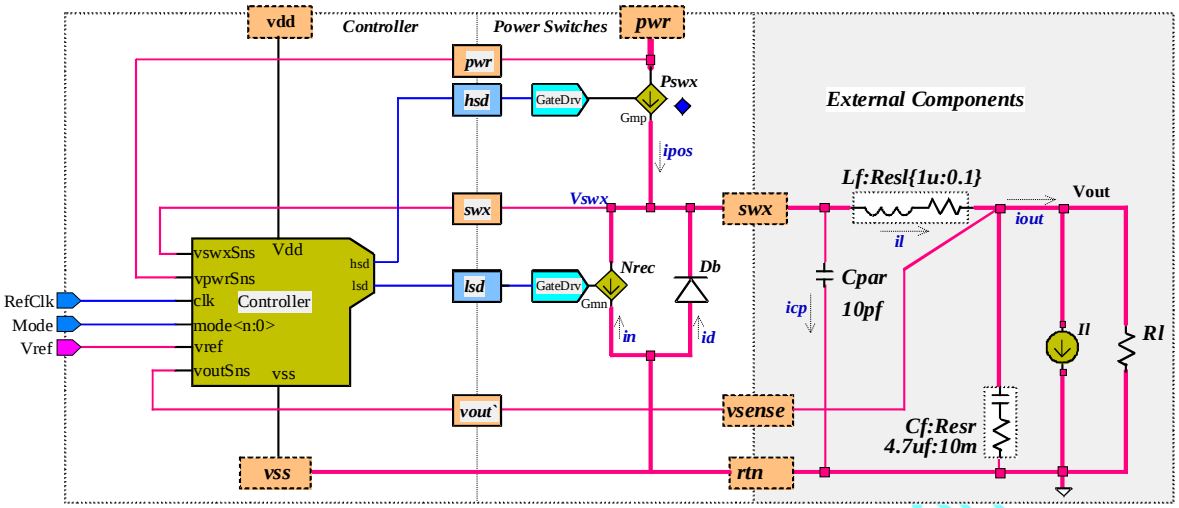
ICDSN	**VerilogA: Buck Switching Regulator** **Top Down System Design Model**	***September 2009***

Description

Verilog-A modeling project for Buck switching regulator system design. Program parameter values for switch rdson and transient time allow trade-off for switch controls. Multiple control techniques implemented to investigate optimal implementation. Code has automatic mode detection and optimization .

Block Diagram



Features

- Voltage Mode Fixed Frequency PWM
- Current Mode Fixed Frequency PWM
- PFM Packet Mode
- Constant Off Time Mode
- Hysteretic Mode
- Async. or Sync. Rectifier Modes
- PWM pole/zero placement Parameters

Pin Descriptions

Power Pins;

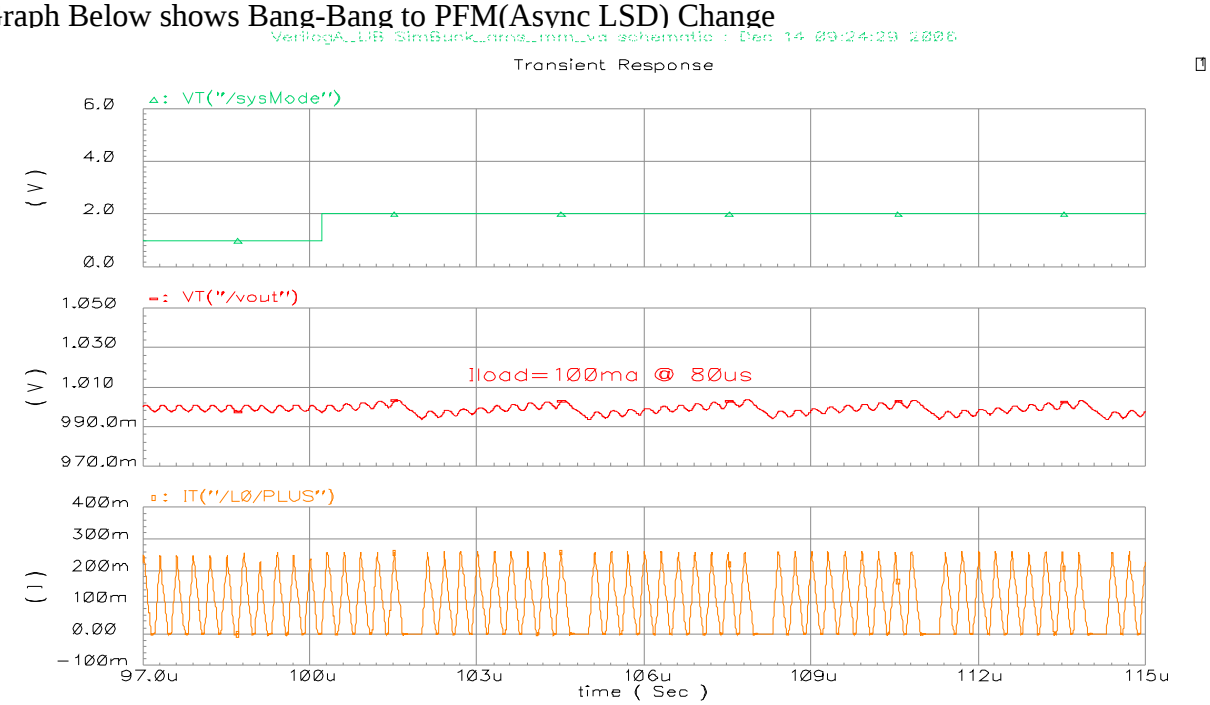
PWR – Power Switch Input Voltage
VDD – Logic Power
SWX – Power Output
RTN – Power Return
VSS – Logic Return

Logic Inputs

CLK – Reference Clock for PWM
MODE – Controller Mode Controls
REF – Voltage Regulation Reference

Simulation Results

Graph Below shows Bang-Bang to PFM(Async LSD) Change



Graph Below Shows PFM to Fixed Frequency Change