Description

This Verilog-A model emulates control modes for Buck Switching Regulators and is designed for use in top down power management system design. Multiple control techniques including; fixed frequency voltage mode pulse width modulation, Pulse frequency modulation, and Bang-Bang(Hysteretic) are available. Control mode may be changed under simulator control. A current limit based on high side switching on resistance has been coded. The model has a disable state and programmable soft start. Test Point pins are included to allow observation of code behavior.

Block Diagram
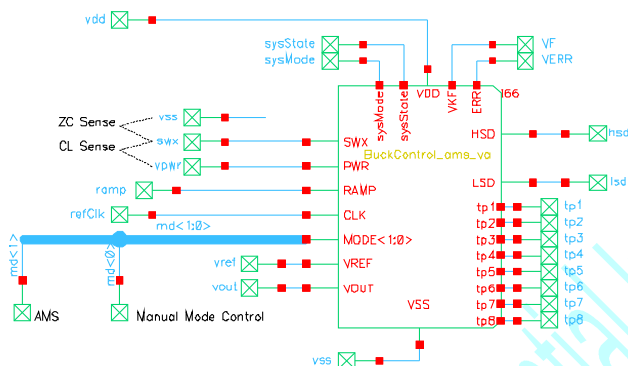
Features

- Integrated Soft Start
- Voltage mode PWM
- PFM Mode
- Hysteretic Mode
- Switching Between Modes via MODE pin
- Test Mode Pins to Observe Code Behavior

Pin Descriptions

Power Pins
   VDD – Bias Power
   VSS – Bias Return
Logic Inputs
   Mode<1:0> Mode Commands
   CLK – System Reference Clock
Analog Inputs
   SWX – Output, CL Sense
   PWR – CL Ref.
   VREF – Reference Voltage
   VOUT – Output Voltage Sense
Logic Outputs
   HSD – High Side Enable
   LSD – Low Side Enable
Auxilary Outputs
   VF – vout sense divider output
   VERR – PWM Error Amp Out
   Tp1-9 – Code -> Test Points
   sysState – Current State(0,1,2)
   sysMode – Current System Mode

Parameters
   pwmKfWz – Kf Feedforward zero
   pwmKfWp1– Kf Feedforward pole
   pwmKfWp2 – Kf Opamp gain pole
   pwmIt – ErrAmp Max Iout
   pwmGm – ErrAmp gm
   pwmRout – ErrAmp Rout
   pwmCc1 – ErrAmp Ccomp
   pwmRc1 – ErrAmp Rcomp
   pwmCc2 – ErrAmpHF roll-off
   verrClpH – ErrAmp Upper Vclamp
   verrClpL –ErrAmp Lower Vclamp
   gkf1– high feedback conductance
   gkf2 – low feedback conductance
   ckf1 – Feedback Feedforward cap.
   vtHys – PFM Voltage Hystersis
   tdSs – Soft Start Time
   vzcTh – Zero Crossing Threshold
   vclSs – Soft Start Current Limit
   vclRun – Normal Current Limit
   hsdBlkDly – Current Limit Delay
   lsdBlkDly – Zero Crossing Delay